

FIG. 1

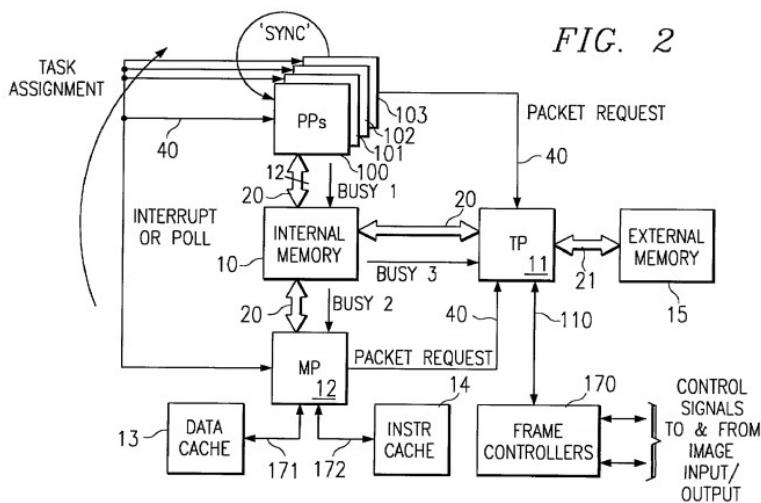
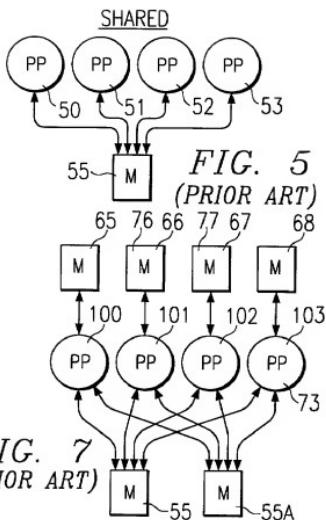
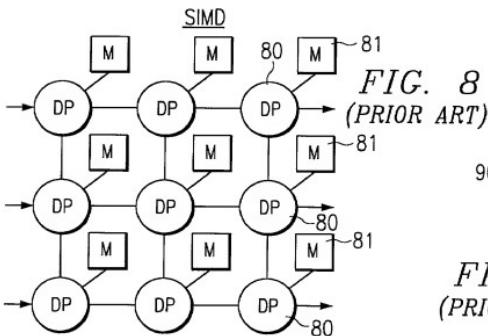
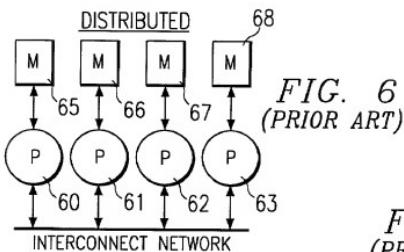
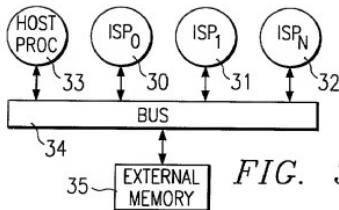
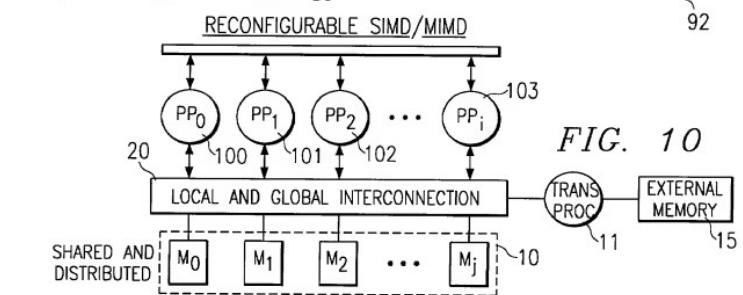
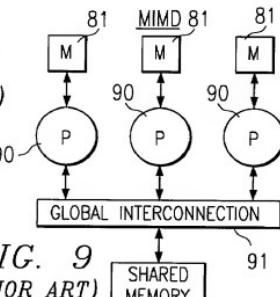


FIG. 2

FIG. 7
(PRIOR ART)

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FIG. 4

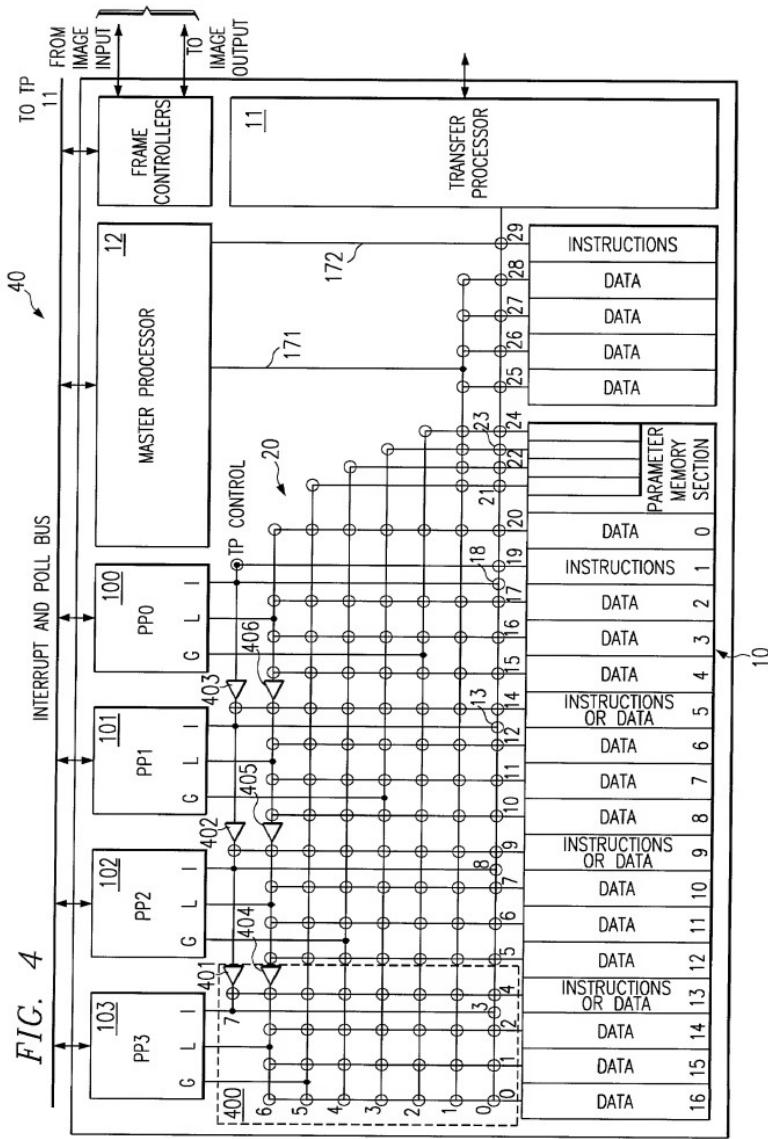


FIG. 11

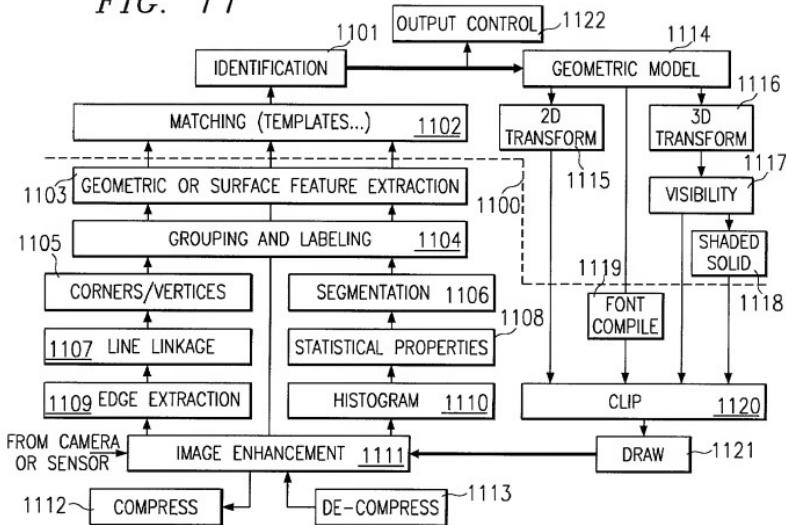


FIG. 12

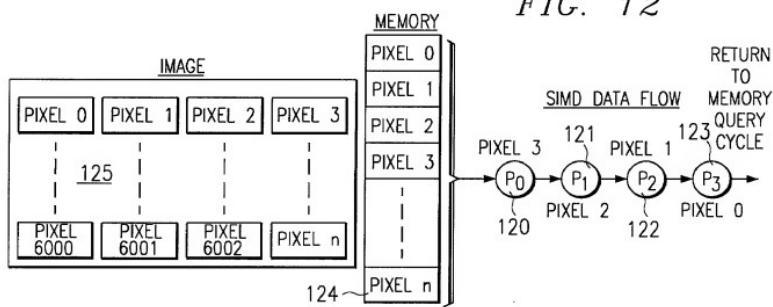


FIG. 13

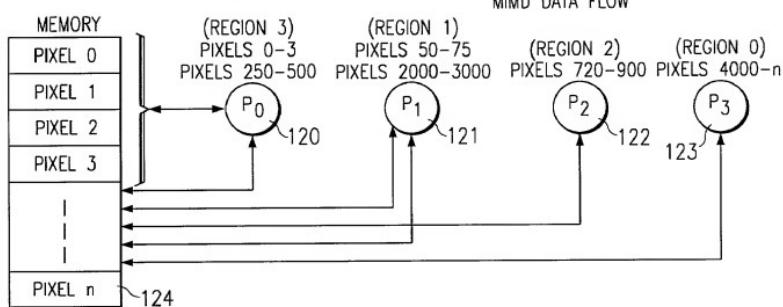


FIG. 14

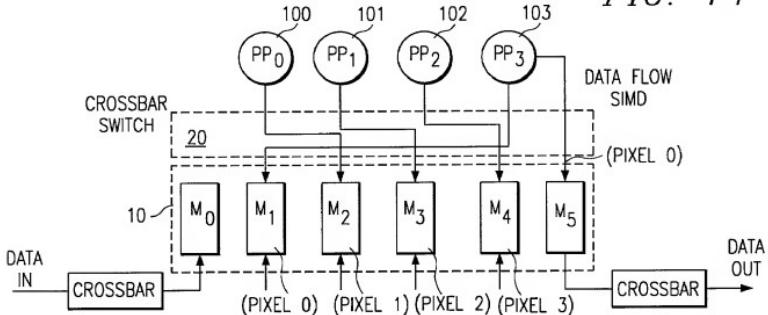


FIG.

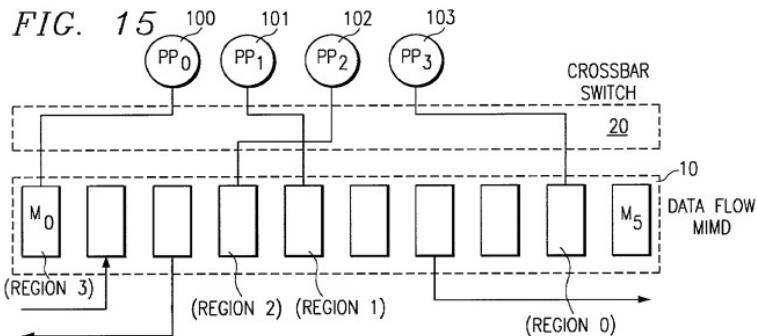


FIG. 16

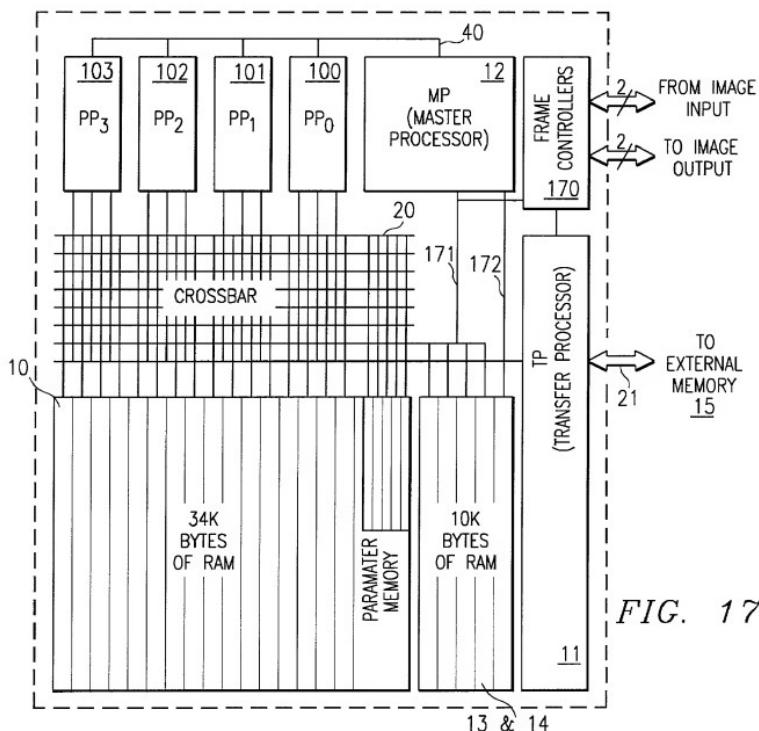
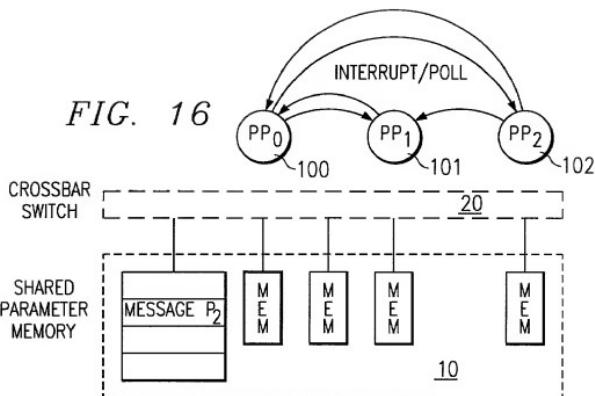
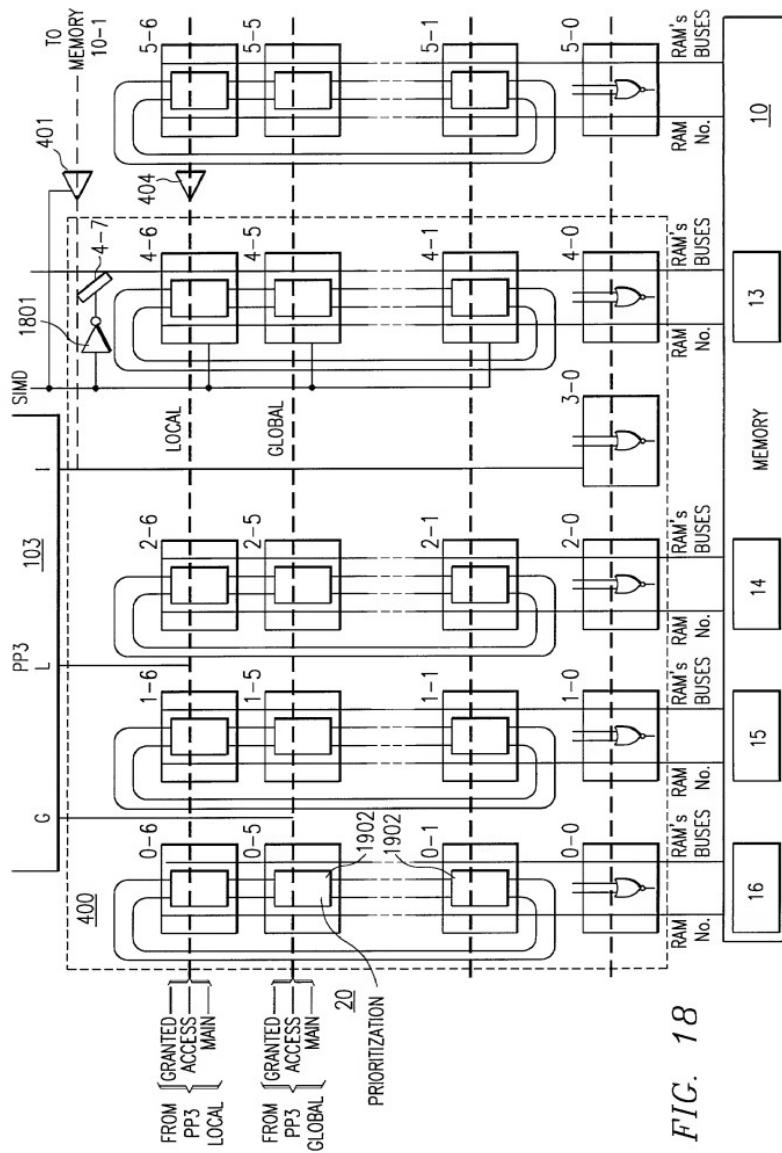


FIG. 17



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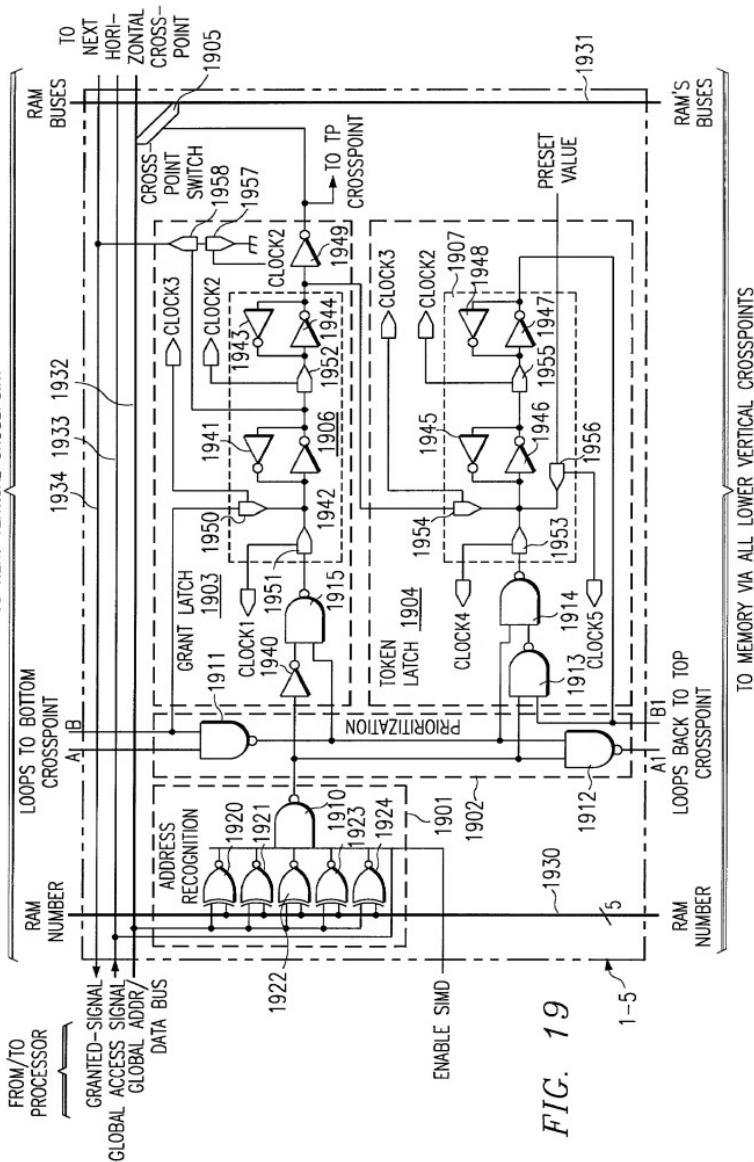
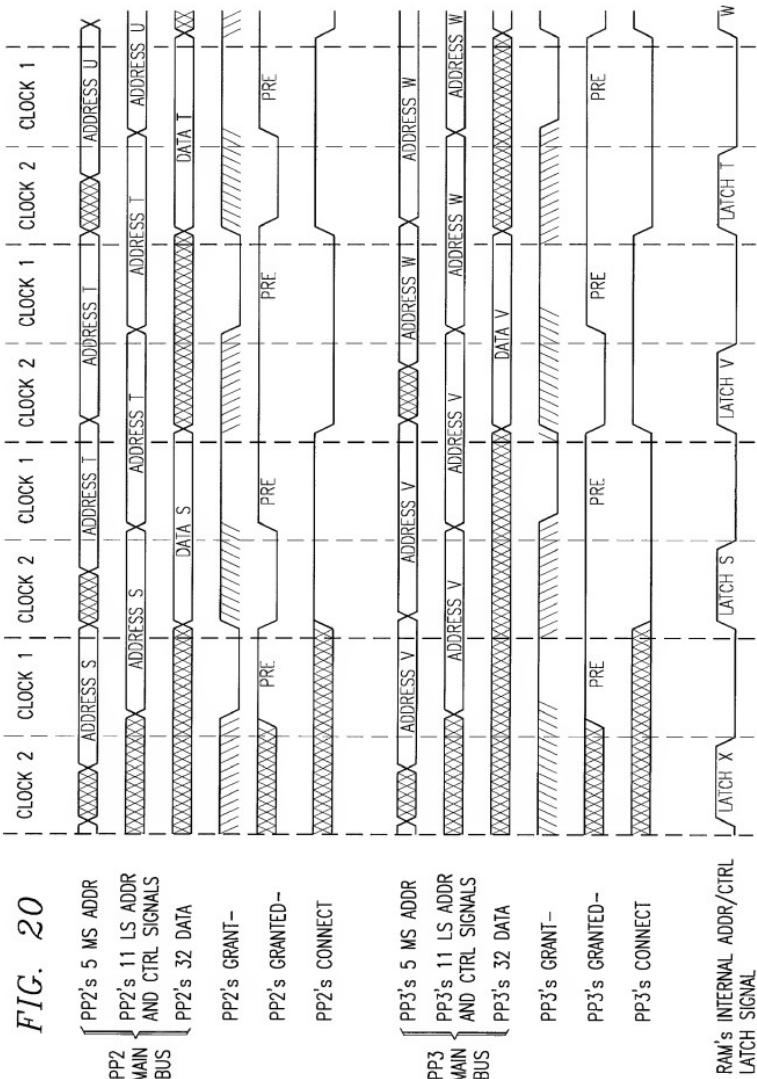


FIG. 20

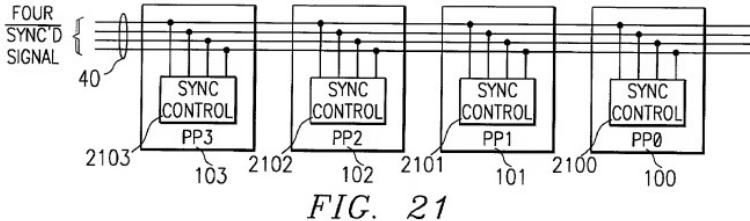


FIG. 21

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>0000	>0800	>1000	>1800	>2000	>2800	>3000	>3800
64 PIXELS	64 PIXELS	64 PIXELS	>1900 >193F	>2100 >213F	64 PIXELS	64 PIXELS	64 PIXELS
>07FF	>0FFF	>17FF	>1FFF	>27FF	>2FFF	>37FF	>3FFF
0	1	2	3	4	5	6	7

NORMAL ARITHMETIC

$$\begin{array}{r}
 >193F - 0\ 0\ 0\ 1\ 1\ 0\ 0\ 1\ 0\ 0\ 1\ 1\ 1\ 1\ 1 \\
 + 0\ 0\ 0\ 1 \\
 = 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 1
 \end{array}$$

$$\begin{array}{r}
 >1940 - 0\ 0\ 0\ 1\ 1\ 0\ 0\ 1\ 0\ 1\ 0\ 0\ 0\ 0\ 0\ 0
 \end{array}$$

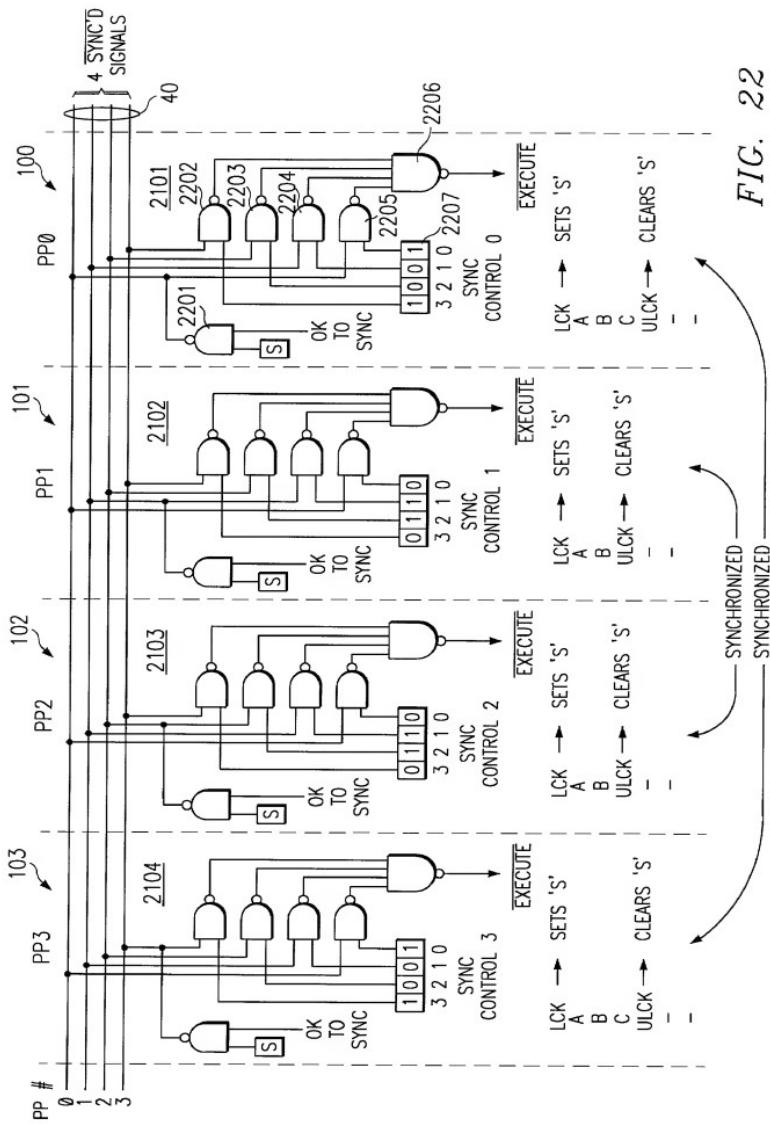
SLICED ARITHMETIC

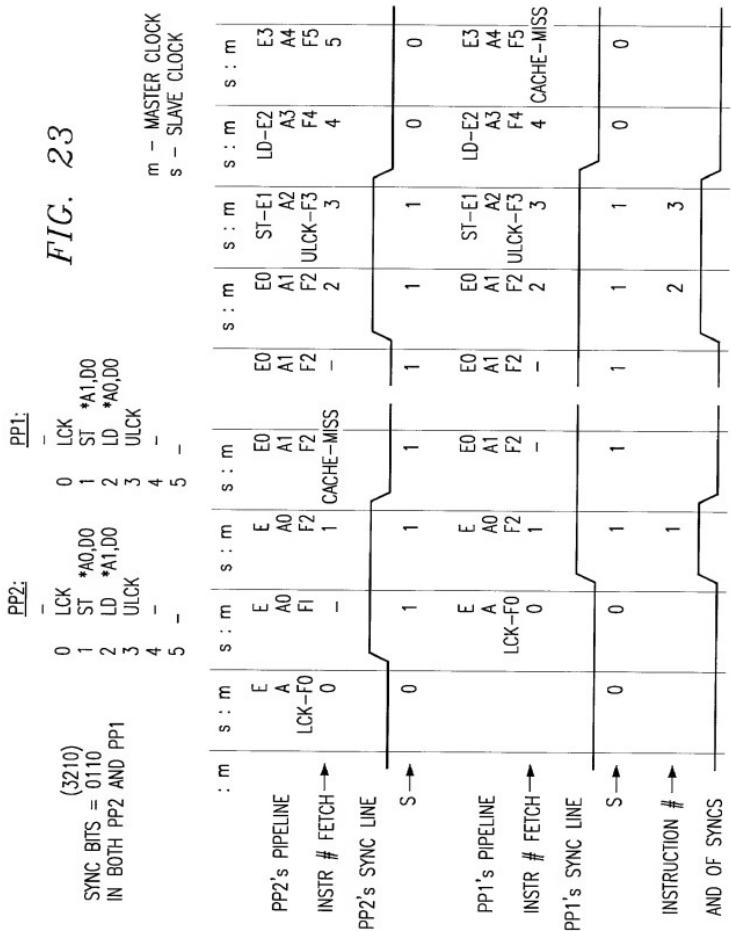
$$\begin{array}{r}
 >193F - \overbrace{0\ 0\ 0\ 1\ 1\ 0\ 0\ 1\ 0\ 0\ 1\ 1\ 1\ 1\ 1}^{\text{SLICE NUMBER}} \\
 (\text{SLICE MASK}) \quad \underbrace{0\ 0\ 0\ 0\ 0\ 1\ 1\ 1\ 1\ 0\ 0\ 0\ 0\ 0\ 0}_\text{CARRY}
 \end{array}$$

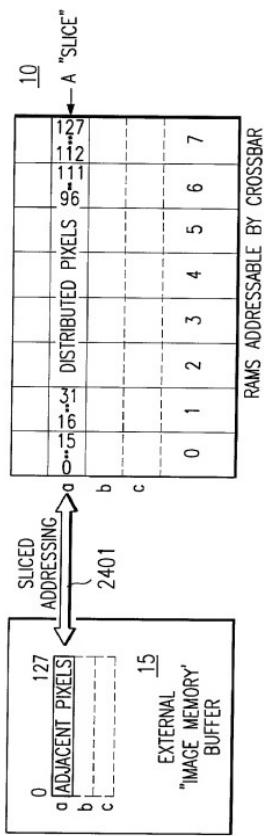
$$\begin{array}{r}
 + 0\ 0\ 0\ 1 \\
 = 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 1
 \end{array}$$

$$\begin{array}{r}
 >2100 - 0\ 0\ 1\ 0\ 0\ 0\ 0\ 1\ 0\ 0\ 0\ 0\ 0\ 0\ 0\ 0
 \end{array}$$

FIG. 27







**FIG. 24
(PRIOR ART)**

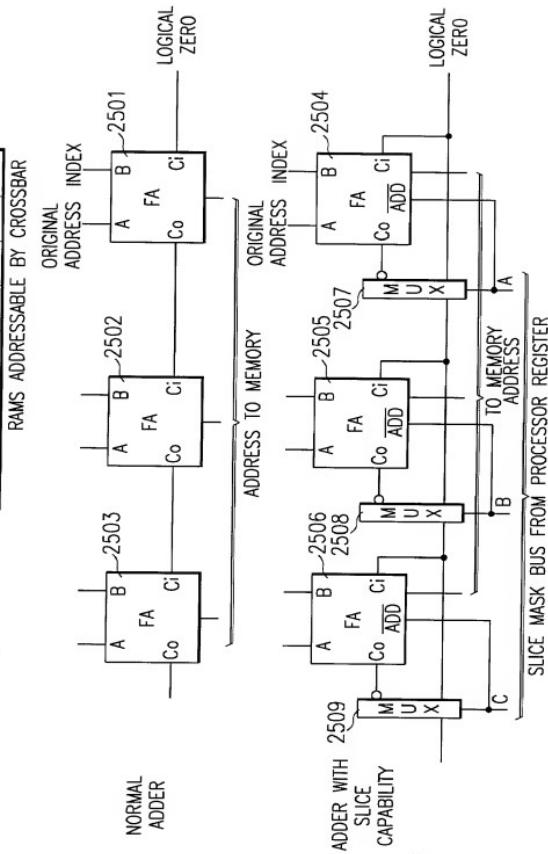


FIG. 28

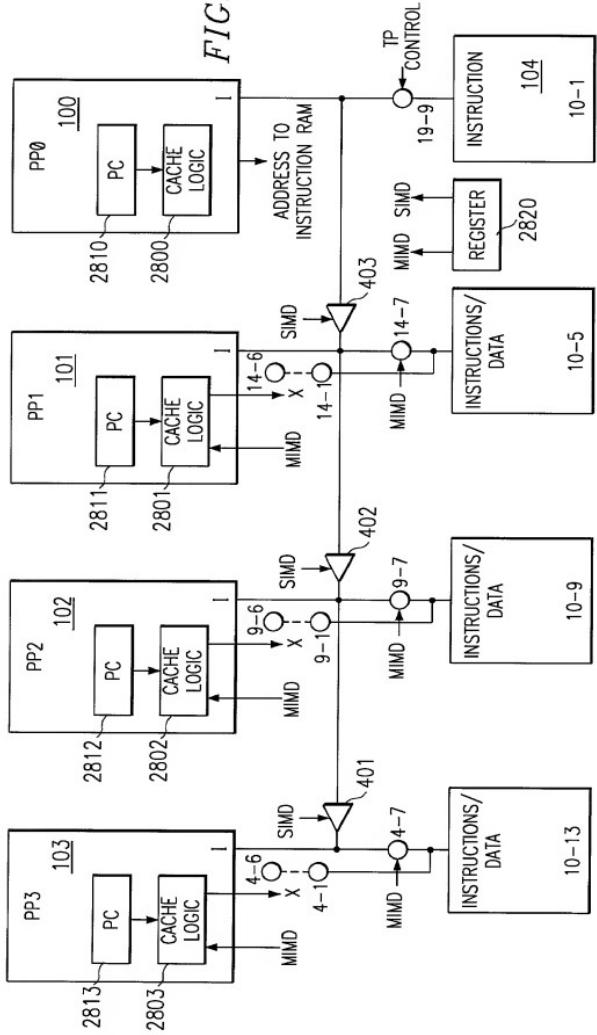
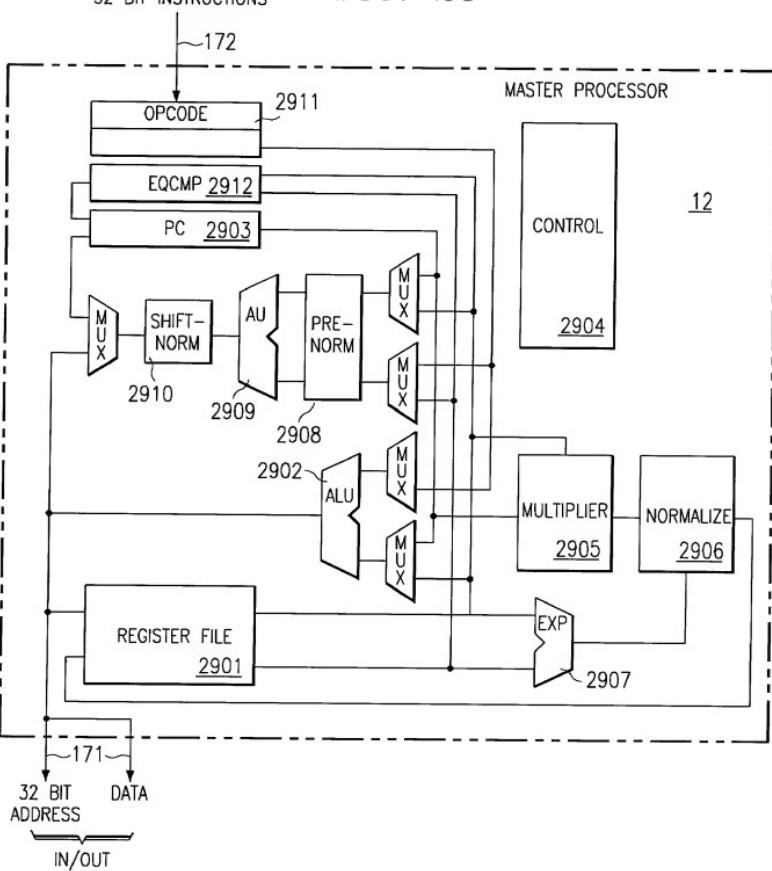


FIG. 29



09875136 - 090601

098753136 "16061

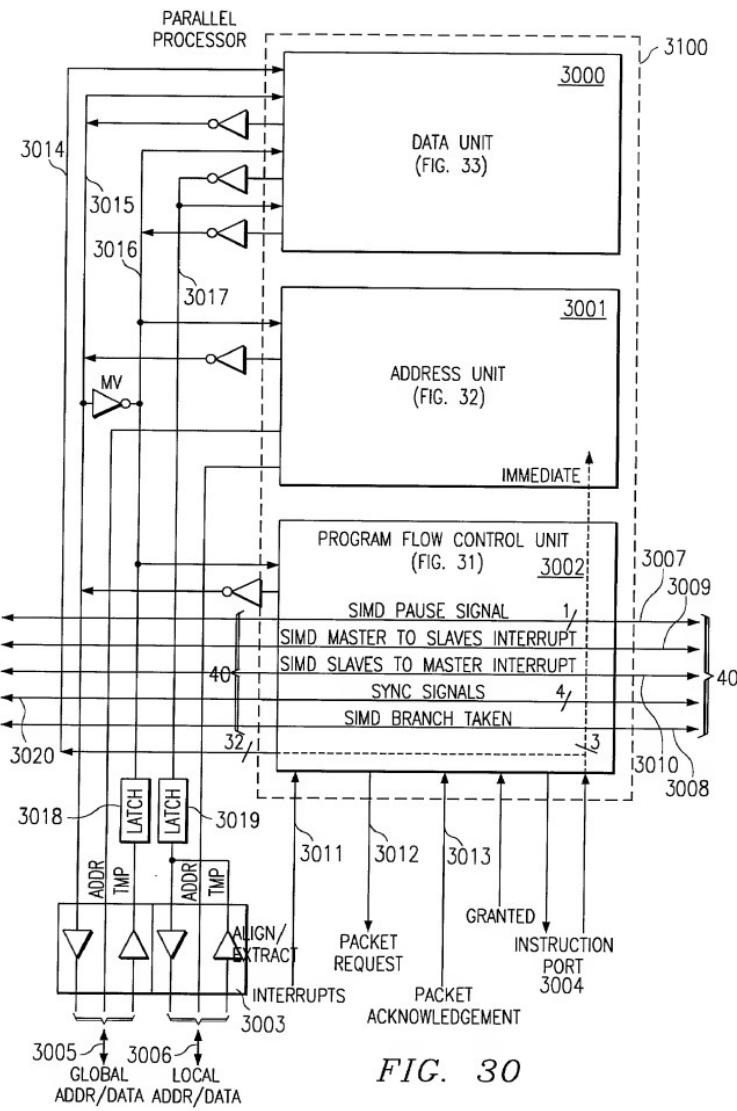


FIG. 30

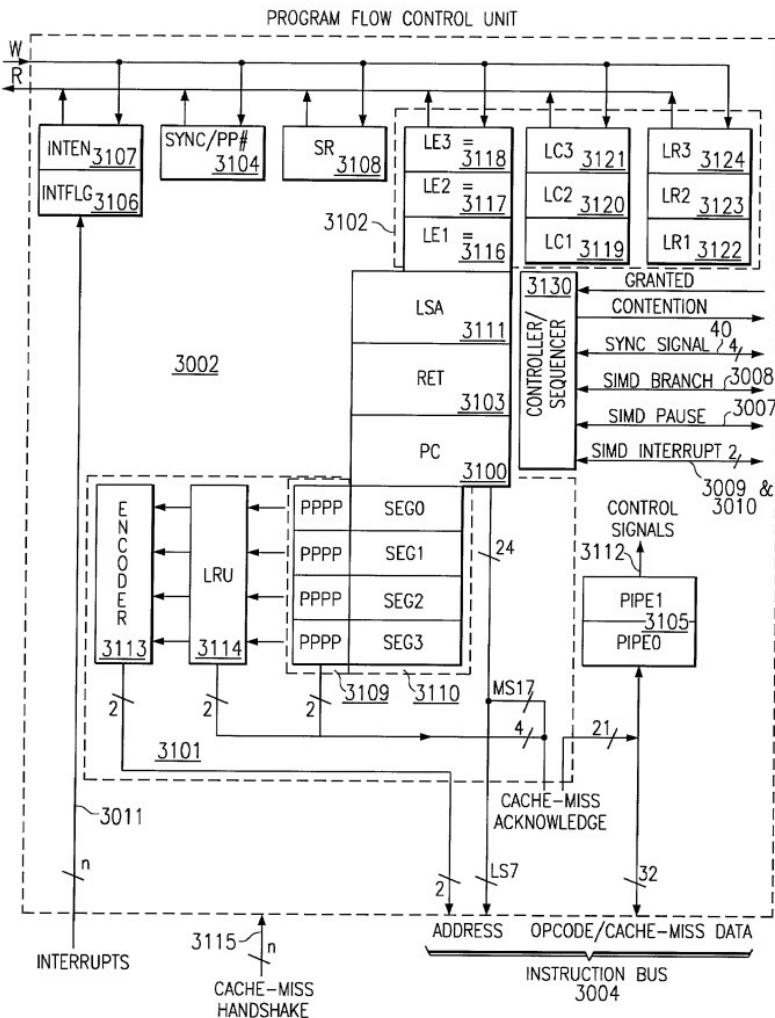


FIG. 31

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T09090 USE A0-A3

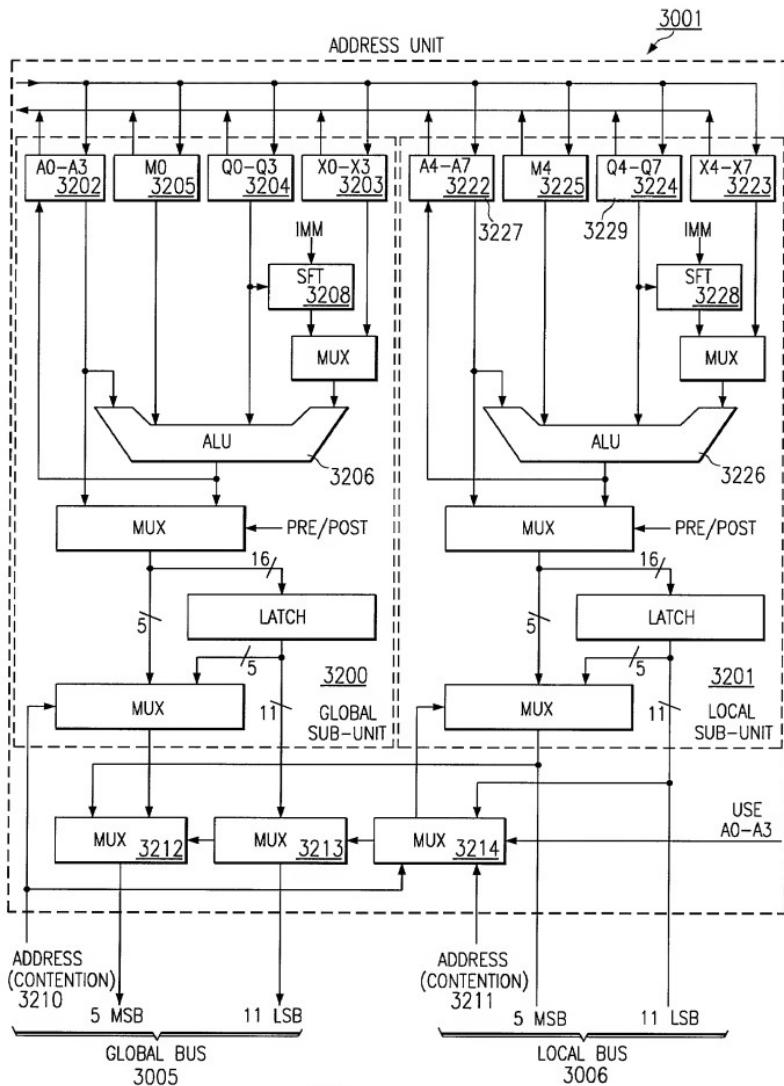


FIG. 32

FIG. 33

3000

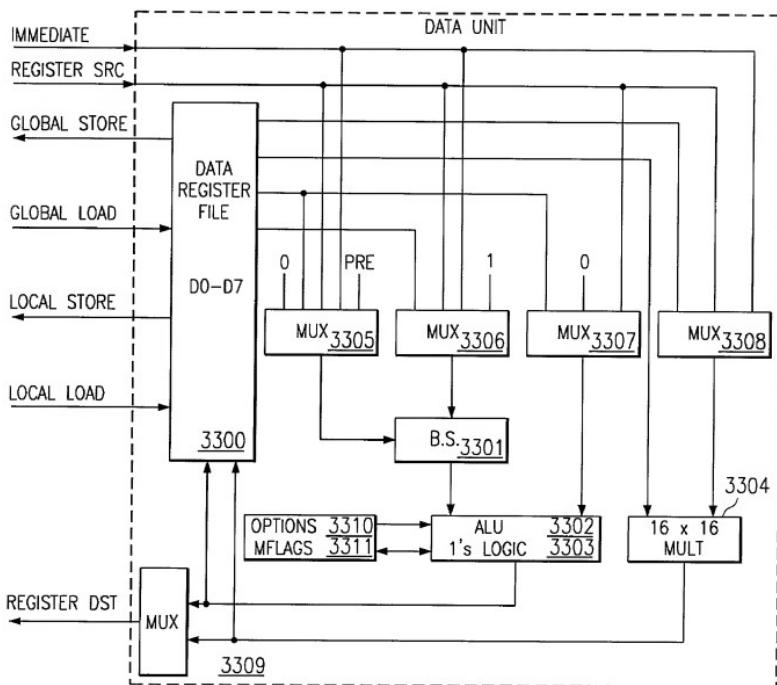


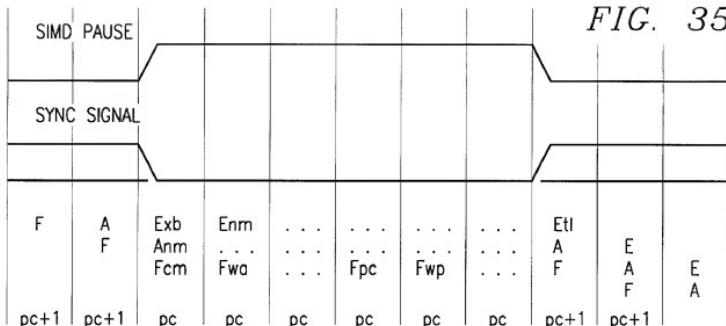
FIG. 34

31

STATUS REGISTER (SR)

0

N C V Z I S MLD CLD 0 0 R U Q P 0



Fcm - CACHE-MISS

Anm - NO MASTER PHASE OF THE ADDRESS UNIT, THUS NO REGISTER MODIFY.

Exb - CROSSBAR ACCESS(ES) OCCUR. STORES COMPLETE TO MEMORY. LOADS COMPLETE INTO TEMPORARY LATCHES, MASTER PHASE OF DATA UNIT OPERATIONS KILLED.

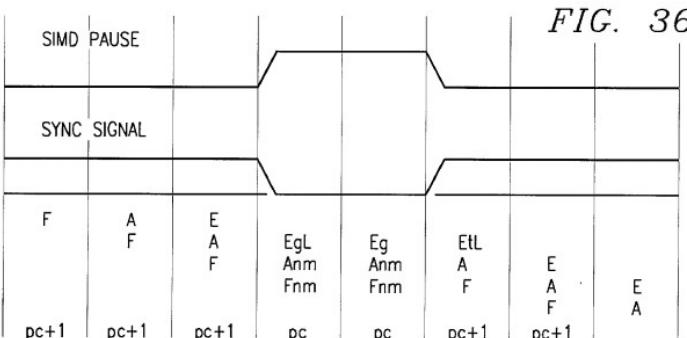
Enm - NO MASTER PHASE OF DATA UNIT.

Fwa - WAIT FOR CACHE-MISS ACKNOWLEDGE FROM TP.

Fpc - TRANSFER PC AND SEGMENT NUMBER TO TP

Fwp - WAIT FOR SUBSEGMENT PRESENT FLAG TO BECOME SET.

Etl - TEMPORARY LATCH DATA (LOADS) COMPLETE INTO DESIGNATION REGISTER(S). DATA UNIT PERFORMS ITS ALU/MPY OPERATIONS.



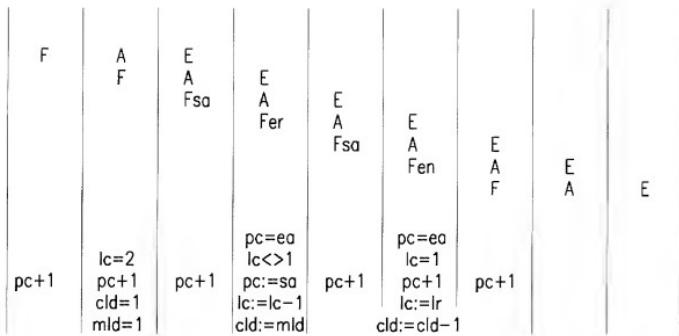
EgL - CONTENTION DETECTED ON BOTH GLOBAL AND LOCAL BUSSES. NO MASTER PHASE IN DATA UNIT.

Fnm - NO MASTER PHASE ON FETCH. PIPE NOT LOADED.

Eg - CONTENTION DETECTED ON GLOBAL BUS. LOCAL BUS TRANSFER OCCURS. STORE TO MEMORY, OR LOAD TO TEMP REGISTER. NO MASTER PHASE IN DATA UNIT.

Etl - TEMPORARY LATCH DATA (LOADS) COMPLETE INTO DESTINATION REGISTER(S). DATA UNIT PERFORMS ITS ALU/MPY OPERATIONS.

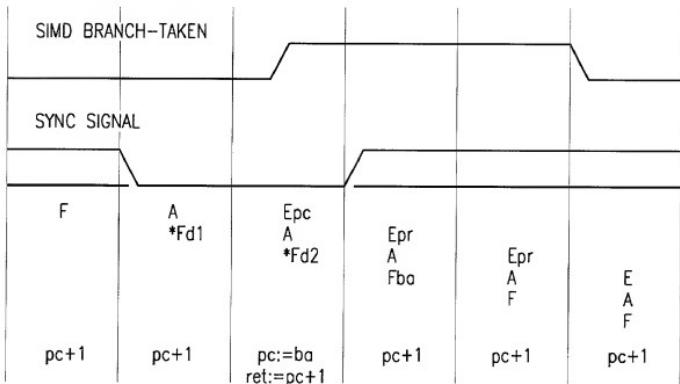
Anm - NO MASTER PHASE IN ADDRESS UNIT. ADDRESS REGISTER NOT MODIFIED.



Fsa - START ADDRESS OF LOOP. PC INCREMENTS NORMALLY.
 Fer - END ADDRESS, REPEAT LOOP. LOOP COUNTER NOT ONE. LOAD PC WITH START ADD.
 Fen - END ADDRESS, NO-REPETITION. LOOP COUNTER IS ONE. PC INCREMENTS NORMALLY.

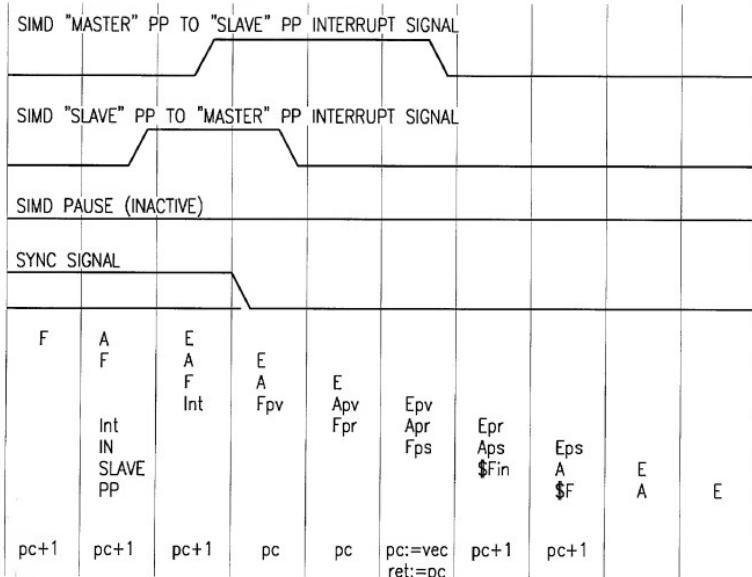
FIG. 37

FIG. 38



Epc - COPY PC+1 INTO RET. LOAD PC WITH BRANCH ADDRESS.
 Epr - PUSH RET IF A CALL. (EITHER Epr CAN PUSH THE RETURN ADDRESS).
 Fd1 - DELAY SLOT 1 INSTRUCTION FETCH.
 Fd2 - DELAY SLOT 2 INSTRUCTION FETCH.
 Fbo - FETCH INSTRUCTION FROM BRANCH ADDRESS.
 * - INTERRUPTS LOCKED OUT.

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Int - INTERRUPT OCCURS.

Fpv - PSEUDO INSTRUCTION. (PC TO RET. VECTOR FETCH INTO PC).

Apv - CALCULATE INTERRUPT VECTOR ADDRESS.

Epv - COPY PC TO RET. FETCH INTERRUPT VECTOR INTO PC.

Fpr - PSEUDO INSTRUCTION. (PUSH RET).

Apr - CALCULATE STACK PUSH ADDRESS.

Epr - PUSH RET ONTO STACK.

Fps - PSEUDO INSTRUCTION. (PUSH SR).

Aps - CALCULATE STACK PUSH ADDRESS.

Eps - PUSH SR ONTO STACK. CLEAR S, I AND CLD BITS IN SR.

Fin - FIRST INSTRUCTION OF INTERRUPT ROUTINE.

\$ - SYNC, INTERRUPTS AND LOOPING DISABLED UNTIL AFTER SR HAS BEEN PUSHED.
NEITHER OF FIRST TWO INSTRUCTIONS OF INTERRUPT ROUTINE MAY BE A LCK.

FIG. 39

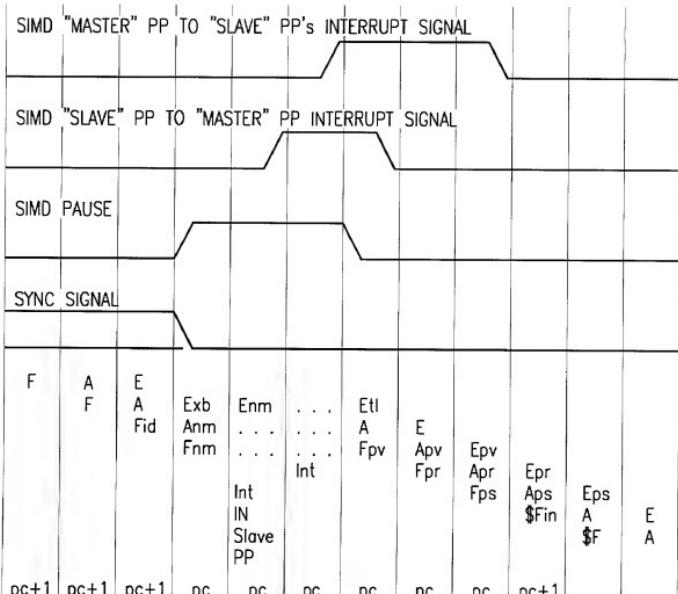
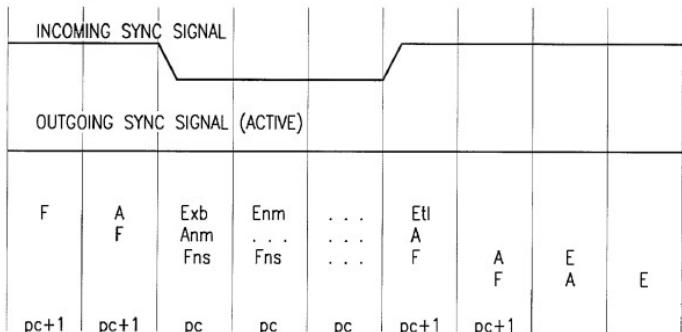


FIG. 40

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FIG. 41



Eqs = NO SYNC CONDITION PIPE NOT LOADED PC UNALTERED

Ann = NO MASTER PHASE IN ADDRESS UNIT ADDRESS REGISTERS NOT MODIFIED

ExB - CROSSBAR ACCESS(ES) OCCUR. STORES COMPLETE TO MEMORY. LOADS COMPLETE INTO TEMPORARY LATCHES. MASTER PHASE OF DATA UNIT OPERATIONS KILLED

From = NO MASTER PHASE IN DATA UNIT

ETM - NO MASTER PHASE IN DATA UNIT.
ETL - TEMPORARY LATCH DATA (LOADS) COMPLETE INTO DESIGNATION REGISTER(S).
DATA UNIT PERFORMS ITS ALU/MPY OPERATIONS.

LOADS: (ASSUMING NO SIGN-EXTENSION)

FIG. 42

SOURCE DATA:				BYTE NO.			
				3	2	1	0
		0000h	=	D	C	B	A
		0004h	=	H	G	F	E
DESTINATION				? ? ? ?	(REGISTER)		
16-BIT				32-BIT			
OP.	ADD.	LOADS...	REG VALUE	OP.	ADD.	LOADS...	REG VALUE
LD	0000h	0 0 B A	0 0 B A	LD	0000h	D C B A	D C B A
LDU	0002h	- - - -	0 0 B A	LDU	0004h	- - - -	D C B A
LD	0001h	- - - B	? ? ? B	LD	0001h	- D C B	? D C B
LDU	0003h	0 0 C -	0 0 C B	LDU	0005h	E - - -	E D C B
LD	0002h	0 0 D C	0 0 D C	LD	0002h	- - D C	? ? D C
LDU	0004h	- - - -	0 0 D C	LDU	0006h	F E - -	F E D C
LD	0003h	- - - D	? ? ? D	LD	0003h	- - - D	? ? ? D
LDU	0005h	0 0 E -	0 0 E D	LDU	0007h	G F E -	G F E D

STORES:

SOURCE DATA: = D C B A (REGISTER)

DESTINATION DATA: = 3 2 1 0
BYTE NO.
-----0000h = ? ? ? ? (MEMORY)
0004h = ? ? ? ?

OP.	ADD.	16-BIT		OP.	ADD.	32-BIT		REG VALUE
		STORES...	0000h 0004h			STORES...	REG VALUE	
ST	0000h	0 0 B A	? ? B A ? ? ? ?	ST	0000h	D C B A	D C B A ? ? ? ?	
STU	0002h	- - - -	? ? B A ? ? ? ?	STU	0004h	- - - -	D C B A ? ? ? ?	
ST	0001h	- - A -	? ? A ? ? ? ? ?	ST	0001h	C B A -	C B A ? ? ? ? ?	
STU	0003h	- B - -	? B A ? ? ? ? ?	STU	0005h	- - - D	C B A ? ? ? ? D	
ST	0002h	- A - -	? A ? ? ? ? ? ?	ST	0002h	B A - -	B A ? ? ? ? ? ?	
STU	0004h	B - - -	B A ? ? ? ? ? ?	STU	0006h	- - D C	B A ? ? ? ? D C	
ST	0003h	A - - -	A ? ? ? ? ? ? ?	ST	0003h	A - - -	A ? ? ? ? ? ? ?	
STU	0005h	- - - B	A ? ? ? ? ? ? B	STU	0007h	- D C B	A ? ? ? ? D C B	

FIG. 43

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ADD WITH SATURATE		MAXIMUM	TRANSPARENCY
ADDM	D0, D1, D2	SUBM	D0, D1, D2
MRGM	D2, D3, D2	MRGM	D0, D1, D2
D0 = 89 23 CD 67	+D1 = 01 AB 45 EF	D0 = 89 23 CD 67	D0 = 89 23 CD 67
D2: = 8A CE 12 56	MFLAGS: = ?? ?? ?? ?3	-D1 = 01 AB 45 EF	(-)D1 = 23 23 23 23
D2: = 8A CE FF FF	MFLAGS: = ?? ?? ?? ?5	D2: = 88 67 88 67	(= 66 00 8A 44)
D2: = 8A CE 12 56	D3: = FF FF FF FF	MFLAGS: = ?? ?? ?? ?5	MFLAGS: = ?? ?? ?? ?4
D2: = 8A CE FF FF		D0 = 89 AB CD EF	D0 = 89 23 CD 67
		D1 = 01 AB 45 EF	D2 = 87 65 43 21
		D2: = 89 AB CD EF	D3: = 89 65 CD 67
<hr/>		<hr/>	
COLOUR EXPANSION		COLOUR COMPRESSION	GUIDED COPY
LD *A0, MFLAGS	MRGM D0, D1, D2	CMPM D0, D1, D2	LD *A0, MFLAGS
MFLAGS = XX XX XX X6		D0 = 89 23 CD 67	MRGM D0, D1, D1
D0 = 11 11 11 11		(-)D1 = 89 89 89 89	
D1 = 88 88 88 88			
D2: = 11 88 88 11		(= 00 89 44 CD)	
MFLAGS = XX XX XX XC		MFLAGS = ?? ?? ?? ?8	
D0 = 89 23 CD 67			
D1 = 87 65 43 21			
D2: = 87 65 CD 67			

FIG. 44

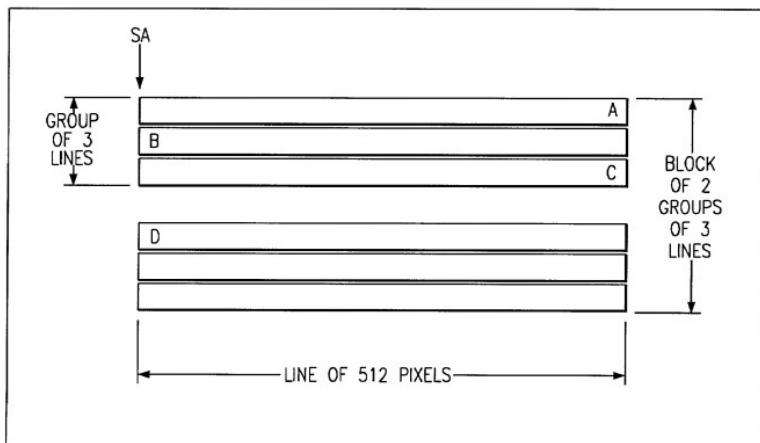
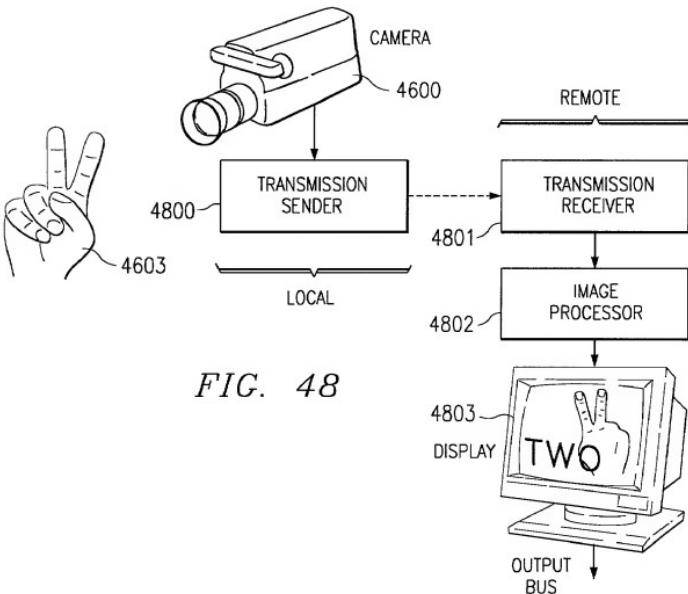
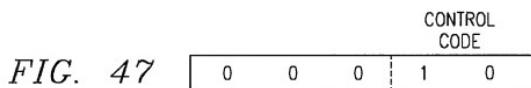
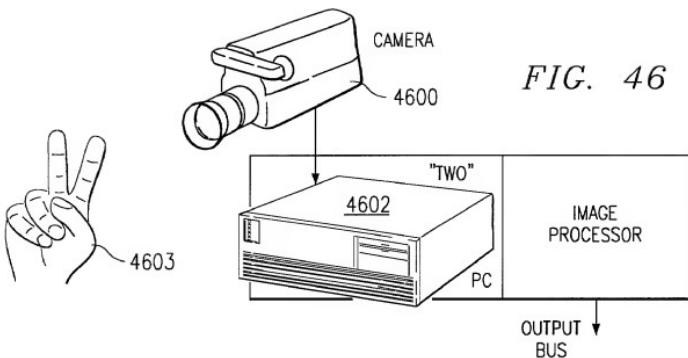
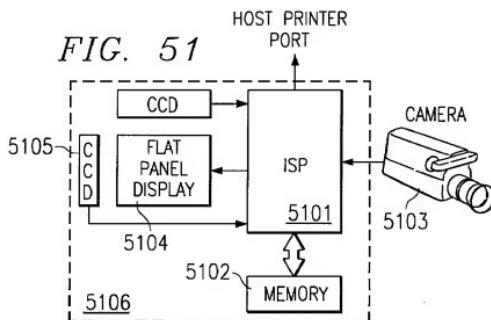
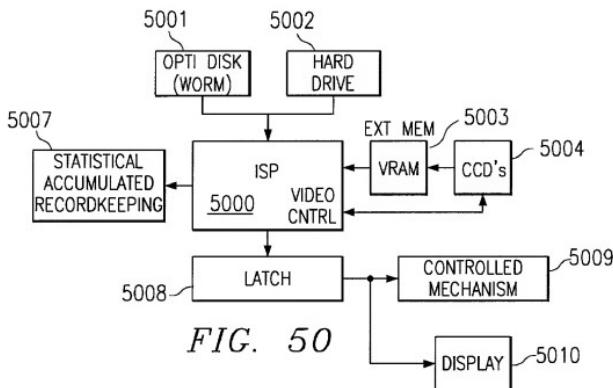
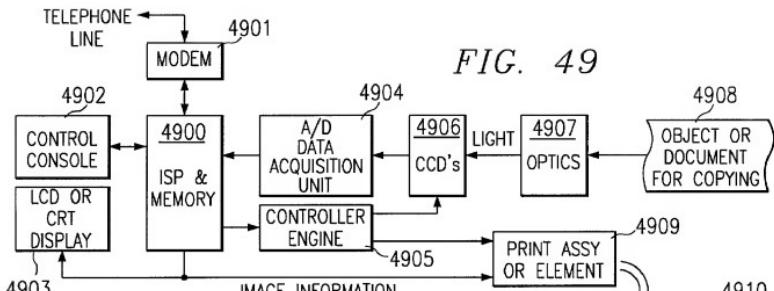


FIG. 45



0909075135 "00"



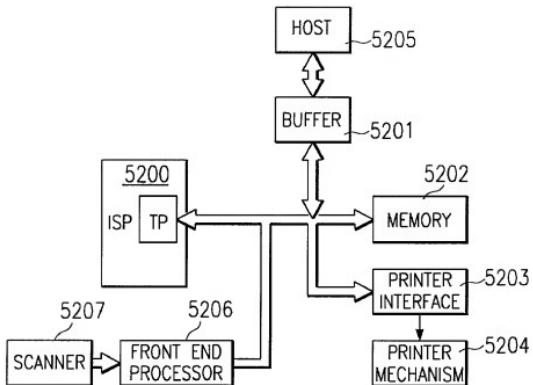


FIG. 52

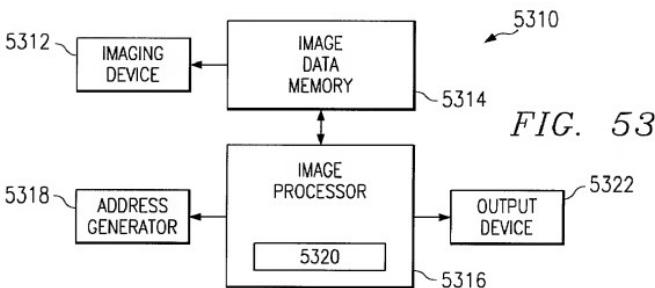


FIG. 53

B93751.36 • 868683

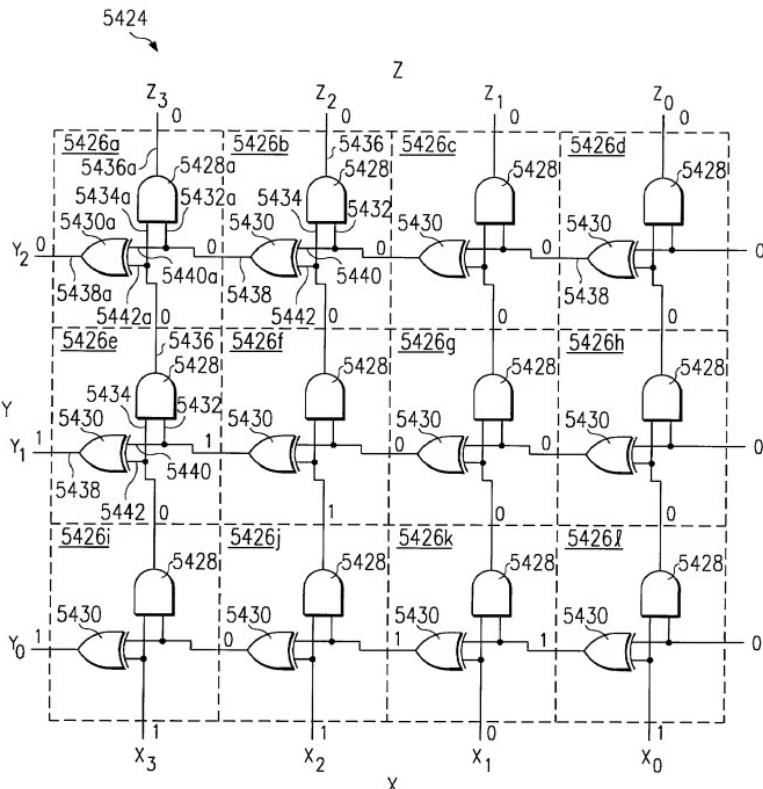
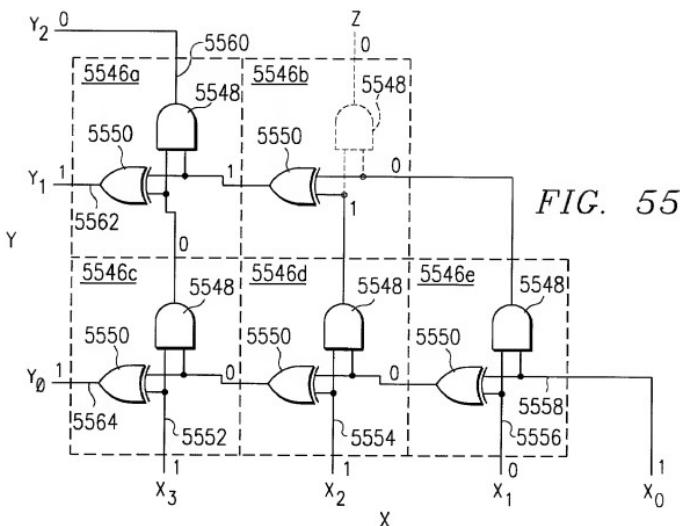
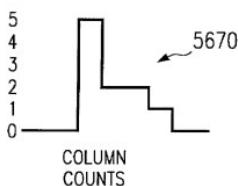
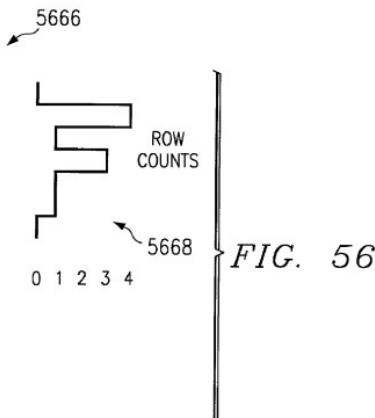


FIG. 54



1	0	0	0	0	0	0	0	0
2	0	0	0	0	0	0	0	0
3	0	0	1	1	1	1	0	0
4	0	0	1	0	0	0	0	0
5	0	0	1	1	1	0	0	0
6	0	0	1	0	0	0	0	0
7	0	0	1	0	0	0	0	0
8	0	0	0	0	0	0	0	0
9	0	0	0	0	0	0	0	0
1	2	3	4	5	6	7	8	



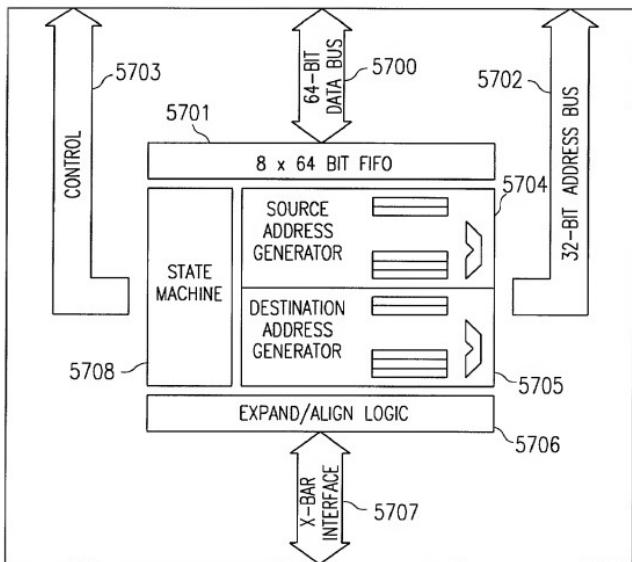


FIG. 57

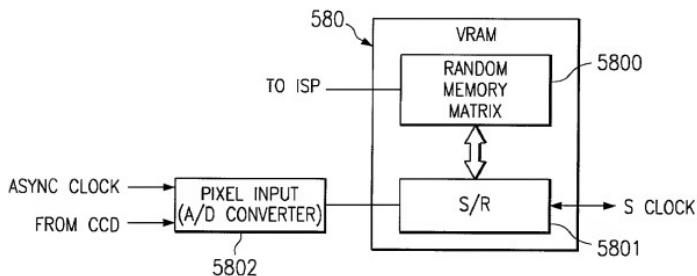
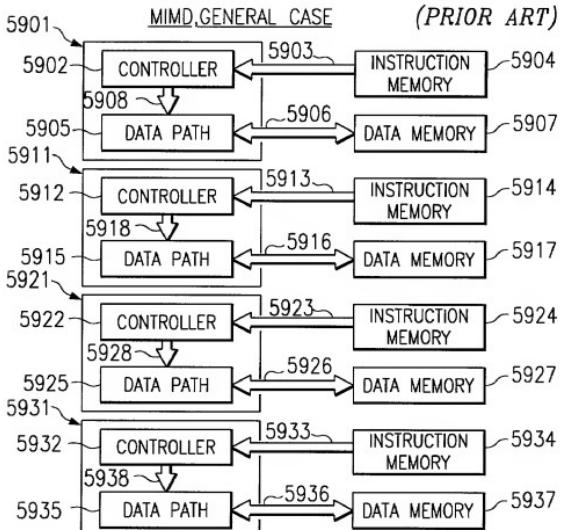
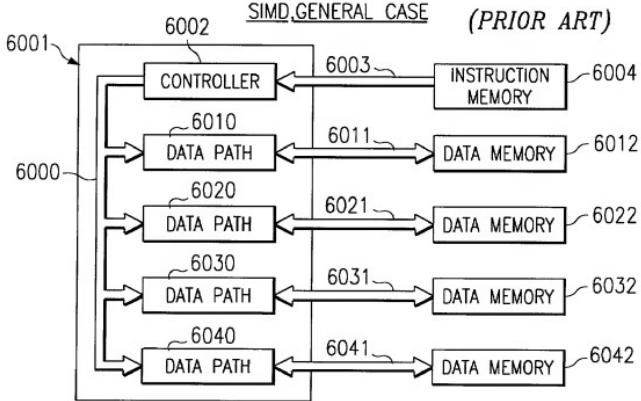


FIG. 58

*FIG. 59
(PRIOR ART)*



*FIG. 60
(PRIOR ART)*



T09090 "9EY54860

FIG. 61

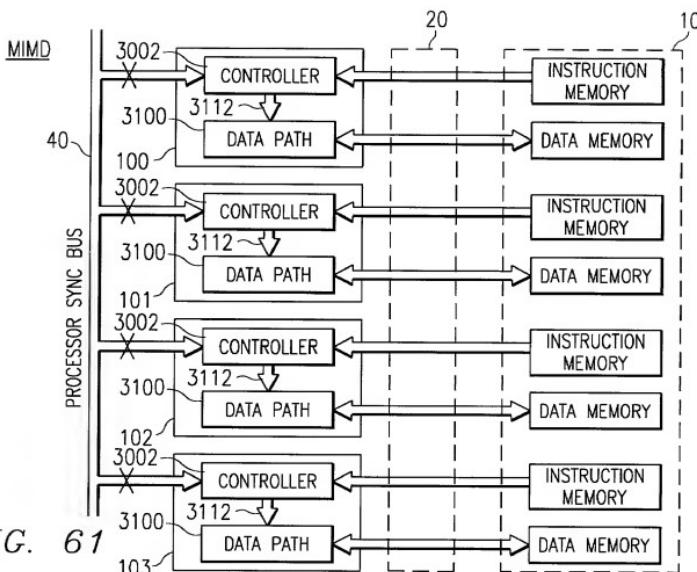
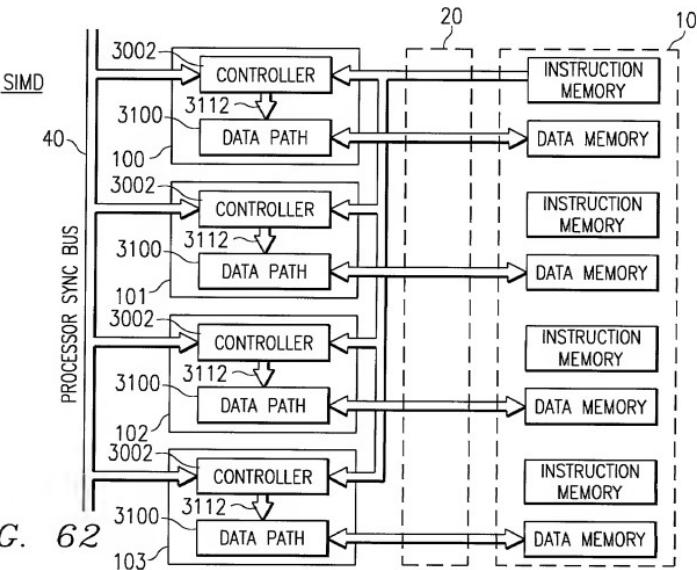


FIG. 62



T09090 "SETS/860

FIG. 63

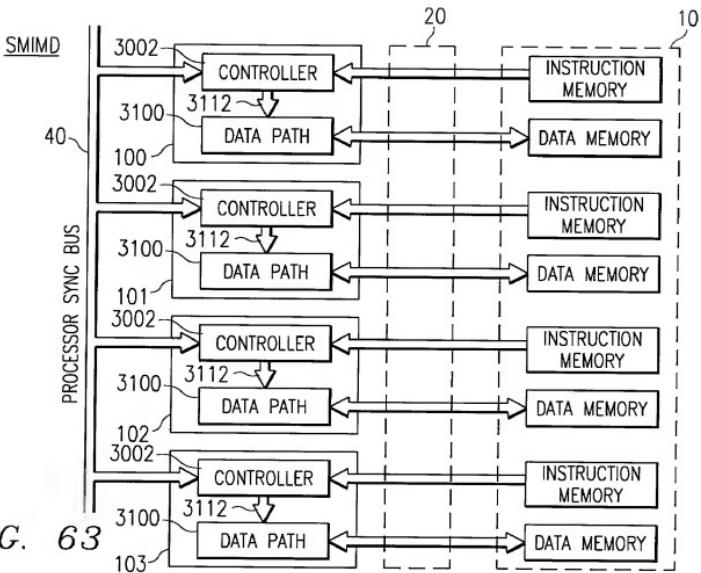


FIG. 64

